In the Specification

At page 1, after the title insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation Application of U.S. Patent Application Serial No. 10/039,456 filed December 31, 2001, entitled "An Improved Method, Structure and Process Flow to Reduce Line-Line Capacitance with Low-K Material," naming Ying Huang and Er-Xuan Ping as inventors, which is a Divisional of U.S. Patent Application Serial No. 09/653,153 filed August 31, 2000, now U.S. Patent No. 6,531,407 which issued March 11, 2003, the disclosures of which are incorporated herein by reference.

The paragraph beginning at line 9 of page 4 has been amended as follows:

In some embodiments of the present invention, multiple levels of interconnects are formed having multiple ~~low-K~~ low-K region structures formed of one or more ~~low-K~~ low-K materials, where the one or more materials can have different insulative properties. In some multiple level embodiments in accordance with the present invention, a single type ~~low-K~~ low-K material is employed for each low-K region, while in some embodiments more than one ~~low-K~~ low-K material and or standard dielectric constant material is employed to form a dielectric region having a dielectric constant less than that which would be obtained if only such standard ~~material~~ materials are employed.

The paragraph beginning at line 6 of page 7 has been amended as follows:

Still referring to Fig. 1, first dielectric stack 50 is shown further encompassing a first etch-stop or protective-barrier layer 30 overlying low-K layer 20. In some embodiments in accordance with the present invention, it is advantageous to employ first protective-barrier layer 30 to prevent outgassing from low-K layer 20 during the subsequent formation of a first standard dielectric constant (K) layer 40. First standard-K layer 40 is depicted in Fig. 1 as being encompassed by dielectric stack 50. In some embodiments, first barrier layer 30 serves primarily in a subsequent process as an etch-stop in addition to or instead of serving as a protective-barrier to prevent the aforementioned out-gassing. Advantageously, where barrier layer 30 encompasses one of the common dielectric materials such as silicon nitride, a silicon oxynitride or silicon carbide, such layer is formed with a thickness in the range of about 3 nm to about 15 nm, although other ~~thickness~~ thicknesses for first barrier layer 30 can be utilized where appropriate, as can other appropriate materials. In some embodiments, barrier layer 30 can be omitted. However, where such layer is present, it will be understood, that the thickness for first barrier layer 30 is dependent on, among other things, the specific material and forming process used for low-K layer 20 as well as the material selected for barrier layer 30. Thus for a first barrier layer 30 encompassing silicon nitride and where first layer 20 is cured hydrogen silsesquioxane (HSQ), a thickness for layer 30 of approximately 3 nm to 8 nm is appropriate and a thickness of approximately 5 nm is typical.

The paragraph beginning at line 2 of page 14 has been amended as follows:

Turning now to Fig. 7, the structure of Fig. 6 is depicted after a second dielectric stack 150 encompassing a low-K constant layer 120, a second barrier layer 130 and a second ~~standard-K~~ standard-K layer 140 are formed. As shown, second low-K material 120 fills first open regions 42 and extends elevationally above first interconnects 76. Typically, second low-K material layer 120 is formed to have a thickness that provides for such layer to extend above interconnects 76 by at least about 100 nm to about 600 nm, although other thickness can be employed. Second low-K material 120 can have the same composition as first low-K material 20 or can be a different low-K material. In one exemplary embodiment of the present invention, first low-K material layer 20 encompasses a carbon-comprising silicon oxide material and second low-K material 120 is a hydrogen silsesquioxane (HSQ) material. It will be noted that after forming second layer 120, such layer can be planarized prior to forming second barrier layer 130 and second ~~standard-K~~ standard-K material 140. However, where second low-K material 120 is formed using a spin-on type material and process, generally, such planarization is not needed to provide an essentially planar structure as depicted in Fig. 7. The forming of second materials 120, 130 and 140 is analogous to the forming of first materials 20, 30 and 40, although the thickness dielectric stack 150 is generally greater than that of first stack 50. For example, where first dielectric stack 50 is formed having a thickness of about 800 nm, second stack 150 will have a thickness of about 1200 nm. However, the materials and methods described for layers 20, 30 and

40 are generally applicable to the forming of second layers 120, 130 and 140 and will therefore not be described again. However, as mentioned for first barrier layer 30, the forming of second barrier layer 130 is optional.

The paragraph beginning at line 7 of page 16 has been amended as follows:

Referring now to Fig. 11, the structure depicted in Fig. 10 is shown at a subsequent processing step where second ~~standard-K~~ standard-K or sacrificial layer 140 is removed and second interconnects 176 are formed. It will be noted that in some embodiments, such forming of second interconnects 176 and removal of second sacrificial layer 140 is accomplished in a manner analogous to that of forming first interconnects 76 and removing first sacrificial layer 40. However, in some embodiments of the present invention, other methods are employed. For example, second conductive layer 170 can be etched using a commonly known plasma etching process to expose portions of second ~~standard-K~~ standard-K layer 140 and layer 140 then subsequently removed using second barrier 130 as an etch stop. Thus it will be understood that the specific method of forming the structure depicted in Fig. 11, nor that of other structures depicted in the other figures herein, is not intended to limit the scope and spirit of embodiments of the present invention.